REMARKS

The Applicants respectfully request reconsideration of this Application. The Applicants originally submitted Claims 1-15 in the Application. The Applicants have previously canceled Claims 4, 9, 14 and 15 and have presently amended Claims 1-3, 5-8 and 10-13. No claims have been added. Accordingly, Claims 1-3, 5-8 and 10-13 are currently pending in the Application.

I. Rejection of Claims 1, 2, 5-8 and 10-12 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2, 5-8 and 10-12 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,726,491 to Tajima *et al.* (Tajima).

Tajima discloses a "tape carrier package" with a conductor pattern formed on the edges of an insulating film package so that a determination can be made as to whether the package has chipped or cracked edges. (Figures 5 and12). The tape carrier package in Tajima provides for an insulating film with a device hole within which a semiconductor chip device is packaged. The semiconductor device is not part of the insulating film, but is a separate component. (Abstract). The insulating film has a number of conductor leads that project beyond the inward edge of the device hole for electrically connecting the semiconductor chip device. (Figure 5). In one embodiment, the tape carrier package provides for a conductive trace to circumscribe the periphery of the insulating film. If the insulating film has a break or crack and the trace loses its conductivity, the tape carrier package can be discarded as defective.

Tajima does not describe a substrate that has an integrated circuit device integral therewith that uses an internal metallization layer to form the interconnects for such circuit. Tajima also does not describe a substrate with an integral integrated circuit device that is electrically isolated from

bond pads coupled by a conductive trace formed by the internal metallization layer. Therefore, Tajima does not disclose each and every element of the claimed invention and, as such, is not an anticipating reference for independent Claims 1 and 10. Because Claims 2, 5-8 and 11-12 are dependent upon Claim s 1 and 10, Tajima also cannot be an anticipating reference for Claims 2, 5-8 and 11-12. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to these Claims.

II. Rejection of Claims 1-3, 5-8 and 10-13 under 35 U.S.C. §103

The Examiner alternatively rejected Claims 1, 2, 5-8 and 10-12 under 35 U.S.C. §103(a) as being unpatentable over the combination of Tajima and U.S. Patent No. 5,563,445 to Iijima, *et al.* (Iijima).

As previously indicated, Tajima does not teach a substrate that has an integrated circuit device integral therewith that uses an internal metallization layer to form the interconnects for such circuit. Tajima also does not suggest a substrate with an integral integrated circuit device that is electrically isolated from bond pads coupled by a conductive trace formed by the internal metallization layer. In short, Tajima does not deal with a device that has another integrated circuit integral thereto. Thus, Tajima fails to teach or suggest the invention recited in independent Claims 1 and 10 and their dependent claims, when considered as a whole.

Iijima does not overcome the deficient teachings or suggestions of Tajima. Similar to Tajima, Iijima describes locating a semiconductor chip over a device hole in a separate substrate, which in this case is a circuit board. Electrode bumps on the semiconductor chip are bonded to conductive leads protruding into the device hole, while dummy bumps on areas of the semiconductor

chip that overlap superimposing areas of the circuit board help to maintain the semiconductor device position. Iijima specifically notes that these dummy bumps are not bonded to a conductive pattern and are only positioned between the circuit board and the semiconductor chip to maintain a specified distance between the two. (Abstract). Unlike the present invention, Iijima does not teach or suggest such a bond pad, or its equivalent, as being connected to a conductive trace. In fact, Iijima specifies the opposite. Iijima also does not describe a substrate with an integrated circuit device integral thereto, but instead describes a separate device that is to be attached to the substrate. Iijima also does not describe or suggest using an internal metallization layer to form the interconnects for a circuit that is electrically isolated from a conductive trace connected to at least two of a plurality of bond pads. Thus, the combination of Tajima and Iijima fails to teach or suggest the invention recited in independent Claims 1 and 10 and their dependent claims, when considered as a whole, and thus fails to establish a *prima facie* case of obviousness with respect to these claims.

The Examiner also rejected Claims 3 and 13 under 35 U.S.C. §103(a) as being unpatentable over Tajima, or Tajima and Iijima, as applied to independent Claims 1 and 10, or, in the alternative over the combination of Tajima and U.S. Patent No. 5,811,874 to Lee, or Tajima, Iijima and Lee. As previously noted, neither Tajima or Iijima teach or suggest a substrate that has an integrated circuit device integral thereto with an internal metallization layer used to form a conductive trace coupled to bond pads where the conductive trace and bond pads are electrically isolated from the integrated circuit device. Lee does not overcome the shortcomings of the combination of Tajima and Iijima. Lee describes semiconductor chip packaging device that includes a lead frame electrically connected to the chip and mechanically supporting the chip. (Abstract). Thus, like Tajima and Iijima, Lee also teaches away from a substrate with an integrated circuit device

integral thereto where the substrate has an internal metallization layer that forms a conductive trace coupled to bond pads with the conductive trace and bond pads electrically isolated from the integrated circuit device. Because Tajima, Iijima or Lee, individually or in any combination, do not teach or suggest the invention recited in independent Claims 1 and 10, dependent Claims 3 and 13, when considered as a whole, are also not obvious and this particular combination also fails to establish a *prima facie* case of obviousness regarding Claims 3 and 13.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 1-3, 5-8 and 10-13 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-3, 5-8 and 10-13.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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